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Chinese Institute of Engineers - Taichung Chapter
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中華民國112年12月

恭賀

國立聯合大學

土木與防災工程學系

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一、 會務動態

中國工程師學會(台中分會)第 53 屆第 2 次理監事會議記錄

時間：112 年 10 月 13 日（星期五）；下午 14 時 00 分

地點：國立聯合大學(八甲校區)土木系館七樓會議室

壹、主席致詞

貳、工作報告(略)

參、開會事由:

一、頒發 53 屆理、監事證書。

二、113 年度工程終身成就獎、傑出工程師獎、傑出工程教授獎、優秀青年工程師獎等公告日期與開始接受推薦期程討論：

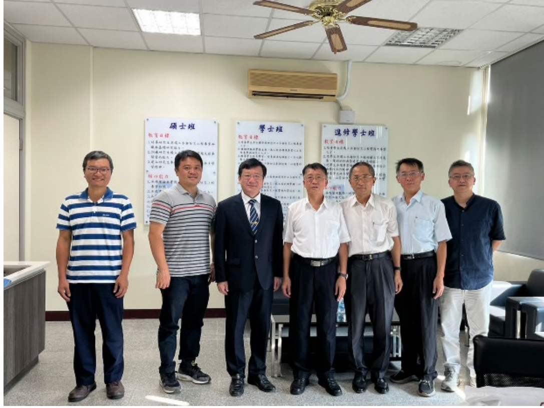
說明：113 年度工程終身成就獎、傑出工程師獎、傑出工程教授獎、優秀青年工程師獎等公告日期因之前有理監事們提出是否提前公告,收件日期另訂，以利

決議：113 年度工程終身成就獎、傑出工程師獎、傑出工程教授獎、優秀青年工程師獎等 12 月初公告、1/15 開始收件、3/15 收件截止

肆、臨時動議(無)

伍、賦歸

第五十三屆第二次理監事會會議照片



與會人員合照

證書頒發

二、專題報導

Heterogeneous Chiplet Integration Ecosystem

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Abstract This paper presents a novel discourse on the heterogeneous chiplet integration (HCI) ecosystem. Since 2017, the Heterogeneous Integration Roadmap (HIR) has replaced International Technology Roadmap (ITRS) for Semiconductors, guiding the semiconductor industry development for over two decades. It is the most significant change in the semiconductor industry in decades. Moore's law is a critical guideline for industrial development. Whether it can continue is an icon of the rise and fall of the industry. Establishing HCI Plug and Play Ecosystem (PPES) is foremost to continue the law since chip scaling (CS) is facing the bottleneck of physical limits. Requiring more articles elucidates a more comprehensive and systematic ecosystem since crucial academic institutions, including IEEE, have just promoted the HCl. This article first reviews the chiplet evolution to explore the topic's connotation. It should help peers to participate in its research and development.

INDEX TERMS: Heterogeneous chiplet integration (HCI), heterogeneous integration roadmap (HIR), International technology roadmap for semiconductors (ITRS), plug and play ecosystem (PPES), chip scaling (CS), Moore's law

I. INTRODUCTION

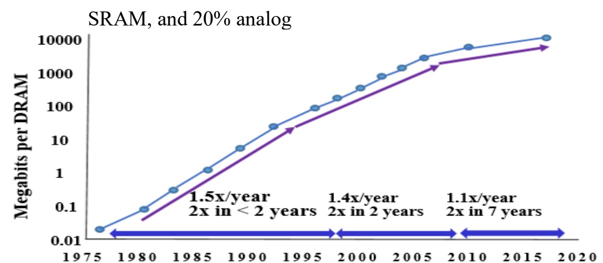
The Semiconductor Industry Association (SIA) officially announced in July 2016 that it would no longer publish the International Technology Roadmap for Semiconductors (ITRS). In March 2017, SIA joined with Semiconductor Research Corporation (SRC), publishing "Semiconductor Research Opportunities: An Industry Vision and Guide" [1] to replace the ITRS that has been used as a guide for the development of the semiconductor industry since 1991 for the Heterogeneous Integration Roadmap (HIR).

Although fabs adopt the techniques such as capacitor deep trench etching, reducing metal wire interconnection, high-k dielectric metal gate (HKMG) transistors that replace polysilicon with hafnium dioxide (H_fO_2) to improve gate capacitance, and the transistor gate structure to prevent current leakage from chips' self-heating and improve chip logic circuit performance. However, the chip scaling's (CS) capacity and density remain downward. Table 1 shows that the performance improvement of the same power consumption accomplished by the contemporary cutting-edge processes, N3E versus N5 and N2 versus N3E, announced by TSMC in CS, is only 18% and 30%, respectively. The chip performance and density improvement achieved only 30% and more than 10% [2]. Fig. 1 reflects the CS of Dynamic Random Access Memory (DRAM) over 40 years. Consequently, fabs require more technological creation to continue Moore's law. It arouses Heterogeneous Chiplets Integration (HCI). HCI refers to integrating separately manufactured "tilelets" into a System-in-Package (SiP). It implies that chiplets with different functions, packaging technologies, and even passive components must be integrated instead of assembling multiple dies in a small package. Its volume after packaging must remain miniaturized [3].

Table 1. TSMC's PPA Changes under Different Processes [2].

	TSMC			
	N5 vs N7	N3 vs N5	N3E vs N5	N2 vs N3E
Power	-30%	-25-	-34%	-25-
Performance	+15%	30%	+18%	30%
Chip Density⋆	?	?	~1.3X	>1.1X
Volume	Q2	H2	Q2/Q3	H2

Note: Chip density of the mixed chips containing 50% of logic, 30% SRAM, and 20% analog



Source: J. Hennessy, ERI Conference, July 2018

Figure 1. Capacity and Density Changes of DRAM Chip Scaling Over 40 Years.

Fig. 2 illustrates HCI and SiP Conceptual Diagram. Some vendors, such as AMD, Intel, Samsung, and Huawei, have

applied HCI to their SiP processors. HIR activities sponsored by the Electronics Packaging Society (EPS), Electron Devices Society (EDS), Photonics Society of the IEEE, Semiconductor Equipment and Materials International (SEMI), and the American Society of Mechanical Engineers (ASME) EPPD Division intend to share the interest with other IEEE technical societies. They regard it as a critical semiconductor technology.

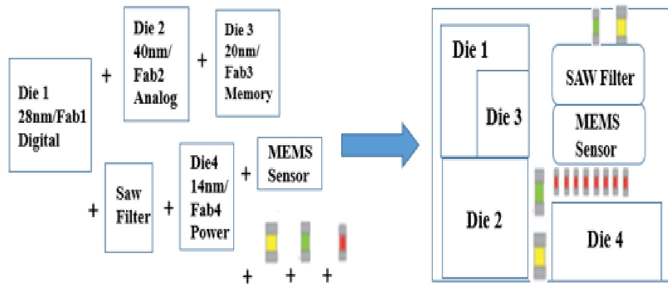


Figure 2. **Conceptual Diagram of HCI and SiP.**

The CS's speed can no longer meet high-end electronic products like AI, high-performance computing (HPC), and 5G in time. HCI will play a leading role in maintaining the law. However, it arouses more complex challenges to the industry. This paper takes the HCI Ecosystem as the core, starting with reviewing chiplet advancement and then clarifying this topic's connotation from a multi-dimensional perspective. It should assist peers in researching related issues on the topic.

II. Chiplet Evolution

Fig. 3 shows that, over a few decades, the packaging evolution from conventional to chiplet-based architecture is a minute change with integrated multi-chip products. The architecture is a new approach to partitioning a System on Chip (SOC) that aligns nicely with advancements in package manufacturing technologies.

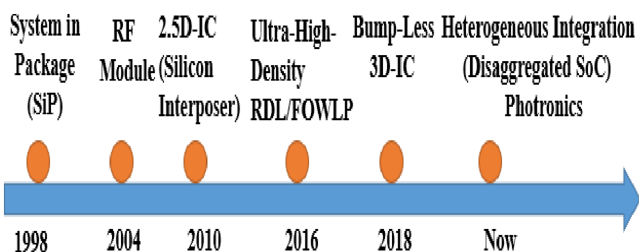


Figure 3. **Evolution of Advanced Multi-Chip(let) Packaging Technologies.**

III. HCI Ecosystem

The impact of heterogeneous integration on the semiconductor industry is not limited to the evolution of packaging and testing technologies. It changes links such as Intellectual Property (IP), IC design, equipment, materials, packaging and testing, norms, communication protocols, and costs, bringing technological changes to the entire semiconductor industry chain. Fig. 4 shows the diagram of the proposed HCI ecosystem.

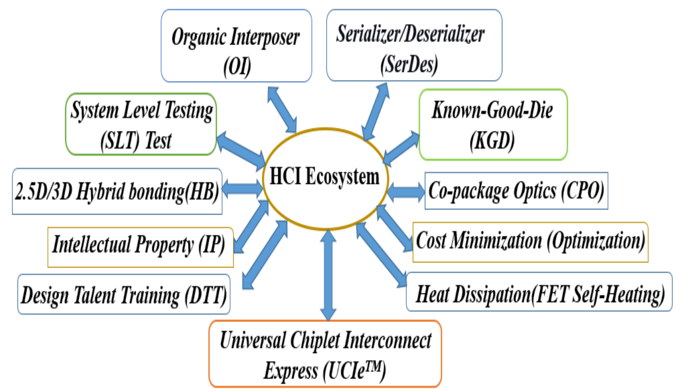


Figure 4. **Diagram of the proposed HCI ecosystem.**

A. Universal Chiplet Interconnect Express (UCIe™)

With the packaging of HCI, IC designers split the various functions integrated by SoC into chiplets and then reintegrate them into a single device. The companies mentioned above, like AMD, have introduced chiplet architecture into their processors. System integration can be homogeneous or heterogeneous. The latter combines chipsets of different processes and materials into one; its fabrication is more complicated than the former. Therefore, it will cover the prior's ecosystem if the engineers can improve the HCI configuration. However, due to the various chiplets produced by major self-developed manufacturers, they need a cohesive interacting mechanism from chip and system designs to packaging and testing.

The UCIe™ [4] standard, also known as the Small Chip Interconnect Industry Alliance, was initiated by Intel and responded to by another nine influential industry players, AMD Arm, Google Cloud, Meta, Microsoft, Qualcomm, Samsung, TSMC, and ASE, in March 2022, aims to help the industry establish a global standard for HCI and enables the concept and technology application to be popularized and promoted faster. It expects to standardize chiplet interconnection. Currently, the alliance has established the UCIe 1.0 criterion.

The specification describes how the physical layer, communication protocols, software models, and compliance tests standardize chip-to-chip interconnects. It enables users to

match chiplets from a multi-vendor ecosystem for Plug and Play and build a general/customized SiP. As an open interconnection constitution, the alliance expects that UCIe™ will facilitate the construction of the chiplets ecosystem. It enables them to realize universal interconnection and an open structure at the packaging level and allows the industry to break through the CS's limitations. All these require multi-dimensional assistance from the industry's supply chain, including Electronic Design Automation (EDA), masks, foundries, Outsourced Semiconductor Assembly and Test (OSAT), Social Network Services (SNS) operators, and material suppliers.

B. Design Talent Training (DTT) and IP

Although the processor's CS cannot meet the HPC's requirements, and the chiplet advantages benefit the chip's cost and package volume, developing the chiplet ecosystem still faces defiances. Moreover, chipset-related design technologies are in the hands of individual manufacturers; it is challenging to train chiplet design talents, which is the key to the success of the chiplet ecosystem development.

Since the Central Processing Unit (CPU) speed is much faster than the read/write rate of the memory, the data flow has become a severe limitation on the overall efficiency, which will cause the CPU to be idle when data is input or output to the memory and severely form an increasingly so-called von Neumann bottleneck problem [5]. Therefore, chip interconnection IP is critical to integrating logic chips and memory into a sub-system architecture through advanced packaging.

C. Hybrid bonding (HB) and Organic interposer

To meet advanced packaging requirements for interconnection density, manufacturers must follow strict process requirements, such as the bonding surface's cleanliness and the material's physical properties. HB technology [6] uses the mixed interface of dual Damascene copper and silicon oxide (SiO_2) as the whole area's bonding medium and electrical connection. It can achieve wafer-to-wafer alignment. However, the interconnection wires' small size and high density increase the difficulty of alignment accuracy. HB makes interconnection lines and contacts finer, which depends on the equipment, materials, and inspection/measurement, and proposes new solutions for developing hybrid bonding processes.

In addition to environmental considerations, Chip-on-Wafer-on-Substrate-R(CoWoS-R) is replacing silicon with an organic interposer [7] because of its better wire impedance. It increases the device's response speed, energy-saving performance, and passive component integration, like the decoupling capacitor. It is more conducive to integrating high-power chips.

D. Serializer/Deserializer (SerDes)

The US Defense Advanced Research Projects Agency (DARPA) formally approved HCI technology [8] in its internal meeting. Influential players in the semiconductor industry, such as Intel (Intel), Advanced Micro Devices (AMD), and Xilinx, introduced it in their products. However, each company's chiplets, and even the materials and packaging methods, produced in closed-loop, need more communication protocols, leading to confining their designs only for their products. The chiplet's miniaturized improvement benefits from setting open technical standards and common operating platforms in the industry.

The first technical challenge is the communication interface standard between chiplets, such as bandwidth, power consumption, interface area, connection density, cost, the pros, and their specific applications using different process chiplets. *SerDes* is a device that uses one or more differential signals to transmit a large amount of data between point-to-point to eliminate many parallel communication bus interfaces, large areas, high cost, enormous power consumption, and complex frequency calibration. It converts high-bit communication signals between parallel and serial communications modes. The *Serializer* converts the parallel input signal into a serial signal; the *Deserializer* transforms the serial signal back to a parallel signal. Although SerDes'es disadvantage is occupying space on the circuit board, its IP helps R & D save time and expenses. Hence, considering serial and parallel interfaces is essential. Serial interfaces, such as conventional *SerDes*, Extremely Short Range (XSR), and Ultra-Short Range (USR) SerDeses [9], must be concerned because most audio-visual signals still support parallel signal interfaces. The emergence of SerDes enables engineers to convert parallel into serial signals for long-distance transmission. Taking automotive applications

as an exampl e, the head unit and the central control instrument panel's mutual transmission guarantee communication quality. Their common advantages are their few connections and interfaces, small areas of the interposer and individual chiplets, and low connection density. XSR and USR are new interfaces for chip -to-chip communication with better frequency bandwidth and energy-saving performance.

Regarding the parallel interfaces, beamline Bunch of Wires (BoW), Advanced Interface Bus (AIB), and High Bandwidth Memory (HBM) [9] is the focus. They are chip-to-chip transmission interfaces. HBM's BoW and the advanced interface bus use clock-forwarding data parallel transmission, similar to Double Data Rate Synchronous DRAM (DDR SDRAM). These interfaces have many I/Os connections and requirements for the interposer's performance. Fig. 5 illustrates the concept of SanDes'es transmission.

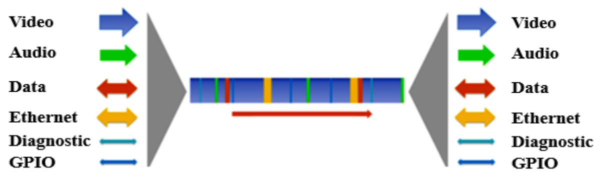


Figure 5. Schematic Diagram of SanDes Differential Signal Transmission.

Moreover, due to the other exceptional performance pursued by the interface, the material and performance requirements of the interposer are different. Three commonly used interposer materials are silicon, organic like epoxy resin and filler, and glass core. The interface with high connection density needs to be processed by silicon semiconductor equipment. Although its bandwidth performance is excellent, the cost is high, and the design and production are complicated. On the other hand, even though beamlines are currently a solution with lower power and higher density; however, if the bandwidth exceeds 400Gb/s per millimeter (mm), they must also turn to silicon interposers. The current organic interposer density has significantly increased. The bump density may reach 40~80μm, and the wire density is 5μm, gradually approaching the performance of the silicon interposer. The performance of the glass core interposer is between the above two and is a more cost-effective choice. In particular, the glass core's Through Glass Via (TGV) has a smaller aperture and a closer pitch, which can connect with the redistribution layer (RDL).

E. Two and half-and three-dimensional (2.5D/3D) Packaging, SIP and Co-Package Optics (CPO)

The CS has been challenging Moore's law due to its approaching the physical limit. 2.5D/3D packaging is according to some innovative technologies, like Silicon Interposers and *Through Silicon Via* (TSV). Compared with traditional packaging technology, it cross-examines the chip design and simulation and layout tools in technological creation such as:

(1) The heat generation becomes more imploded because of the enormous increase in integration. Heat thermal runaway is a significant issue through 2.5D/3D stacking.

(2) Ensuring mechanical and thermal stress reliabilities during the extension and shrinking of a wafer, silicon interposer, or substrate is essential.

(3) The chiplets' high-frequency signals must satisfy the integrity requirements of timing signals.

On the qubits of quantum computing, it is difficult for the current quantum technology to accommodate a considerable number of qubits in a single structure. Thus, a more feasible manner is to use a few single chiplets to make qubit modules and then integrate them into a complete quantum computing unit. Since quantum cipher is memory computing, it does not have much information exchange between modules. What is required is the entanglement between the qubits on each module and the other module. The appropriate manner is to entangle photons between modules, thereby achieving the property of the interposer to transmit photons in a low-temperature environment with low noise

In SiP, the continuous requirement of computing performance, storage capacity, and increasing I/O bandwidth challenge the I/O power consumption. Because of the enormous growth of network data volume, the Netcom chip's I/O bandwidth is getting higher. However, the traditional transmission medium can no longer bear the heat energy generated when extensive data is transmitted. Hence, it needs to adopt Co-package Optics (CPO) technology to realize it. CPO is a typical heterogeneous integration. Chip developers can achieve more communication bandwidth and transmit data in less time by integrating logic units using the CMOS process and photoelectric and optical components using unique processes through advanced packaging, thereby drastically reducing power consumption.

F. Known Good Die (KGD) and System Level Testing (SLT)

The KGD [10] contributes to the SiP assembly of 2.5D/3D, reducing system cost and size, achieving low power consumption, and creating high-speed data transmission performance while reducing electromagnetic interference (EMI)

The SLT [11] allows the chip designer to simulate the chip operation mode in an environment similar to the chip design to achieve the "Test for Design" purpose. Due to its complexity, the gap between transistor testing and fabricating costs is getting smaller, and the interconnection density between chiplets is constantly scaling. HB used to replace the traditional solder bump interconnect technology becomes arduous to meet the needs. It also challenges wafer testing, such as probe card fabrication. Due to CS, many transistors fail to cover even with 99.5% test fault coverage for Automatic Test Equipment (ATE). The SLT can find faults in the remaining 0.5% of undetected transistors.

As technology evolves, the complexity of SoCs, system-in-packages (SIPs), and software continues to increase. This complexity results in increased asynchronous interfaces, more frequent interactions between power, clock, and temperature domains, and software and hardware. ATE's 99.5% test fault coverage rate is also relatively difficult to achieve. The SLT is simple and more economical for testing complex interfaces. Once the device is in mission mode, it may fail to test.

Another challenge is that device makers face the ever-shorter time-to-market and the high number of defects in new ATE. When process defect rates are high, but manufacturers must expedite shipments, it is challenging to guarantee product quality since it requires detecting defects. SLT enables engineers to increase test fault coverage early in device development. The data achieved can help manufacturers reduce rework and repairs in subsequent links, and attain an excellent yield rate in a shorter time, thereby reducing the time required to market. Although IC designers use cutting-edge CS and packaging technologies, they increase the likelihood of potential failures and new failure modes.

G. Heat Dissipation

In the past, IC designers primarily pursued the goals of performance, power consumption, and area (PPA). Even though the die partitioning of the integrated SoC led to reducing cost, shortening the IC design cycle, and integrating multiple chiplets, it led to a new defiance to deal with heat dissipation after interconnection and chip stacking. It depends on the corresponding design process, methodology, and tool support to adopt. The traditional air-cooling manner that uses fans to remove the heat generated by chips will challenge HCI packaging. Considering new cooling solutions, such as reserving holes on the package for coolants to pass through to enhance the device's heat dissipation efficiency, is indispensable as it allows the coolant to pass through to increase the heat dissipation efficiency. The immersion cooling approach to solving the insufficient fan heat dissipation issue is essential to ecosystem integration.

Furthermore, as the computing and storage performance continues to improve, it drives increasing Input/Output (I/O) bandwidth of the Netcom chip, resulting in greater power consumption. However, the traditional transmission medium can no longer carry extensive data at its rated power consumption level Thus, it introduces Co-package Optics (CPO) [12] heterogeneity that integrates the logic unit using the CMOS process and the optoelectronic and optical components using a unique process. Packaging technology to achieve more communication bandwidth and significantly reduce power consumption when transmitting data is also critical.

H. Cost Minimization (Optimization)

In addition to controlling the process's accuracy and precision for HCI, cost control is also a big challenge. Suppose manufacturers use the foundry's Back End OF Line (BEOL) technology for 2.5D/3D packaging, like the copper process; although the processing accuracy and precision, in that case, are higher than traditional assembly, the cost is positively correlated. In contrast, the traditional packaging throughput is high, which is conducive to cost control. However, processing accuracy and precision, such as line width control and alignment accuracy, are negatively correlated with cost. Finding the optimal solution requires stakeholders' tradeoffs from the entire ecosystem.

In the past, the main goal of SoC design was to optimize the chip's PPA. By contrast, HCI takes system miniaturization as the primary objective of optimizing the device's performance, power consumption, and volume (PPV). In addition, in responding to the early-to-market requirements of high-ranking electronic products, Cost and Cycle Time to Market Cost are crucial elements related to the HCI Ecosystem success; that is, performance, power consumption, volume,

cost, and cycle time to market (PPVCC) is the system's core content, and cost optimization is the core of the core.

IV. CONCLUSIONS

This paper has presented a comprehensive notion originating from the norm, DTT, IP, HB, potential interfaces, packaging, test, and optimal cost to construct an HCI Plug and Play Ecosystem (PPES) for inter-chipsets communication. The concept presented provides a tradeoff to optimize the system's PPVCC. However, limited by developing technologies such as XSR and USR, this study needs to conduct a further investigation later. Implementing a SiP empirical study of the HCI will be future work. The concept presented provides a tradeoff to optimize the system's PPACC. However, limited by developing technologies such as XSR and USR, this study needs to conduct a further investigation later. Conducting a SiP empirical study will be future work.

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Ching-Chih Tsai (2017 Fellow, IEEE) received the Diploma degree in electrical engineering from the National Taipei Institute of Technology, Taipei, Taiwan, in 1981, the M.S. degree in control engineering from National Chiao Tung University, Hsinchu, Taiwan, in 1986, and the Ph.D. degree in electrical engineering from Northwestern University, Evanston, IL, USA, in 1991. He is currently a Life Distinguished Professor at the Department of Electrical Engineering, National Chung Hsing University (NCHU), Taichung. He is a Fellow of IEEE, IET, CACS, RST and TFSA. From 2003 to 2005, he served as the Director of the Center of Research Development and Engineering Technology, College of Engineering, National Chung Hsing University. In 2006, he served as the Director of the Center for Advanced Industry Technology and Precision, National Chung Hsing University. He served as the department chair of the Department of Electrical Engineering, NCHU, from 2012 to 2014. From 2012 to 2016, he served two terms as the President of the Chinese Automatic Control Society (CACS), Taiwan. From 2016 to 2019, he served two terms as the President of the Robotics Society of Taiwan (RST). From 2019 to 2021, he served as the President Elect for IFSA; since 2021, he has served as the IFSA President. Since 2022, he has served as a BoG member of IEEE SMCS. He has published and co-authored more than 600 technical articles. His current research interests include fuzzy control systems, advanced control methods, and intelligent learning control systems with their applications to commercial and industrial products, mobile robots, and intelligent machinery.

三、 其他相關資訊

台中分會網站資訊將持續更新，期望能為台中分會的會員朋友們提供一個分享交流、學習、溝通及傳承的平台，歡迎大家隨時上網瀏覽並提供意見。

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